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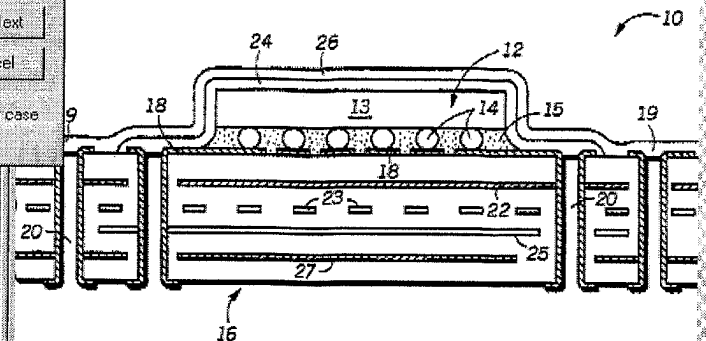
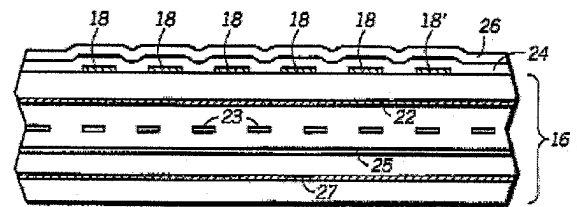
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alloys, and other alloys of these metals; lossy ferrite materials such as Ni ferrite or Mn ferrite, or magnetic oxides; or dielectric materials such as barium titanate, strontium titanate, niobate materials, zirconate materials, or magnetic oxides, among others, which are lossy at the frequencies of the EMI.

DEPR:

Efficiency of shielding is a strong function of the electrical and magnetic properties of the materials used in the shield and the characteristics of the impinging field. Electromagnetic fields can be described by the wave impedance ($Z_{sub.w}$) which is the ratio of the magnitudes of the E- and H-field components ($Z_{sub.w} = E/H$). Field sources which conduct relatively high currents at low voltages are low impedance sources. Such sources may be power supply loops, transformers, and electric motors. Fields radiated from such sources have low $Z_{sub.w}$ values, hence the ratio of E-field to H-field intensity is low. Integrated circuits (ICs) operate at relatively high voltages compared to the currents driven, and as such are considered high impedance signal sources. Such signals have high $Z_{sub.w}$ values due to a high E-/H-field intensity ratio. At large distances, the $Z_{sub.w}$ value from either a low or high impedance

**FIG. 1****FIG. 2**

Details

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KWIC

Details

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Full



US006097080A

United States Patent [19]
Nakanishi et al.

[11] **Patent Number:** **6,097,080**
[45] **Date of Patent:** **Aug. 1, 2000**

[54] **SEMICONDUCTOR DEVICE HAVING
MAGNETIC SHIELD LAYER
CIRCUMSCRIBING THE DEVICE**

[75] Inventors: **Tsutomu Nakanishi**, Tokyo; **Akira Okamoto**, Saitama, both of Japan

[73] Assignees: **Susumu Okamura**; **Takeshi Ikeda**, both of Tokyo, Japan

[21] Appl. No.: **09/171,455**

[22] PCT Filed: **Apr. 23, 1997**

[86] PCT No.: **PCT/JP97/01412**

§ 371 Date: **Oct. 19, 1998**

§ 102(e) Date: **Oct. 19, 1998**

[87] PCT Pub. No.: **WO97/40654**

PCT Pub. Date: **Oct. 30, 1997**

[30] **Foreign Application Priority Data**

Apr. 24, 1996 [JP] Japan 8-127783

[51] Int. Cl.⁷ **H05K 1/00**

[52] U.S. Cl. **257/659; 257/660; 257/661;
257/676; 257/687; 257/700**

[58] Field of Search **257/659, 660,
257/661, 676, 687, 700**

[56] **References Cited**

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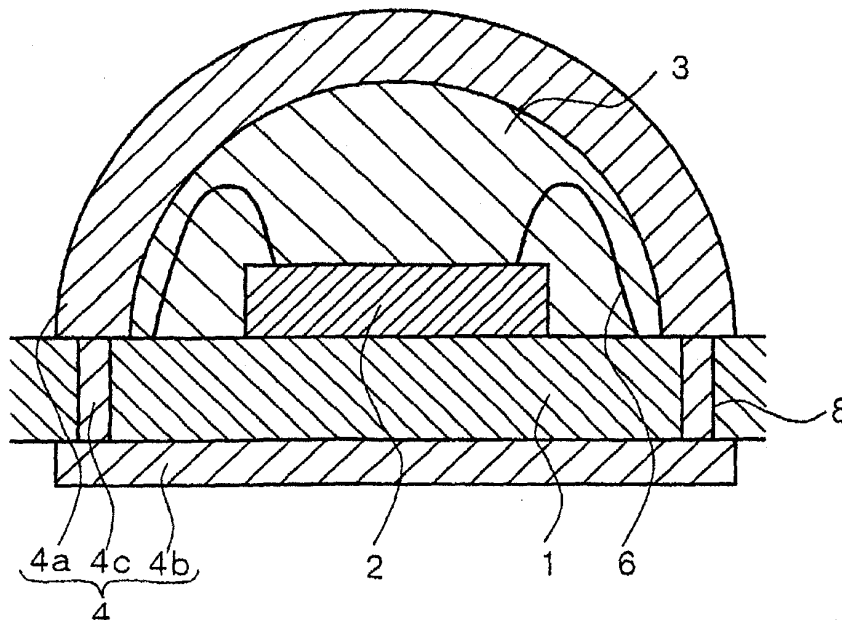
Primary Examiner—Fetsum Abraham

Attorney, Agent, or Firm—Dellelt and Walters

[57] **ABSTRACT**

It is the object to minimize a magnetic influence, on the outside, of a semiconductor chip which is formed on a substrate includes inductor conductors. A semiconductor chip 2 including inductor conductors is mounted on a substrate 1 and a plurality of through holes 8 are formed in the area on the outside of the mounting position. Shielding members 4 are formed on the chip mounting side and the opposite side of the substrate 1 and in the through holes 8 so as to cover the semiconductor chip 2 with the shielding members 4 from both sides of the substrate 1. Therefore, magnetic fluxes from a circuit formed on the semiconductor chip 2 do not leak out from the shielding members 4, but circulate inside the shielding members 4.

6 Claims, 3 Drawing Sheets



BSPR:

The first type includes those substrates which are made primarily of resins, such as a resin plate and a laminated plate obtained by laminated-molding of prepregs which are prepared by drying after impregnating the base material with varnish of the thermosetting resin. The substrates of the first type are most widely used because they have the principal characteristics required for the substrates for wiring boards, such as having superior electric insulation. On the other hand, the high density of the contemporary semiconductor chips generates substantial heat therein and as a result, an escape for such heat has become a great concern. In addition, the noise level becomes annoying unless a magnetic shield is provided. In these regards, it has been recognized that those first type substrates suffer from a lack of heat releasing capability and magnetic shield effect as well.

BSPR:

The second type includes those made of a metal plate as a core extending in the middle of the board and being referred to as a metal core board. The specific structure and performance of the metal core boards are extensively disclosed, for example, in IPC Standard 1985 by The Institute for Interconnecting and Packaging Electronic Circuits and the Hewlett-Packard Journal (August 1983). The substrates of the second type display a superior property regarding the heat releasing capability and the magnetic shield effect. However, they have an inherent disadvantage in securing electric insulation particularly between the leads and the metal core which are located very close to each other. This is particularly true with the LCC (Leadless Chip

United States Patent [54]

Higuchi et al.

[11] Patent Number: 4,835,598
[52] Date of Patent: May 30, 1989

[54] WIRING BOARD

[57] Inventors: Tetsu Higuchi; Toshiyuki Yamaguchi; Takashi Kawanishi, all of Kadoma, Japan
[71] Assignee: Matsushita Electric Works, Ltd., Osaka, Japan
[21] Appl. No.: 82,381
[22] Filed: May 14, 1987

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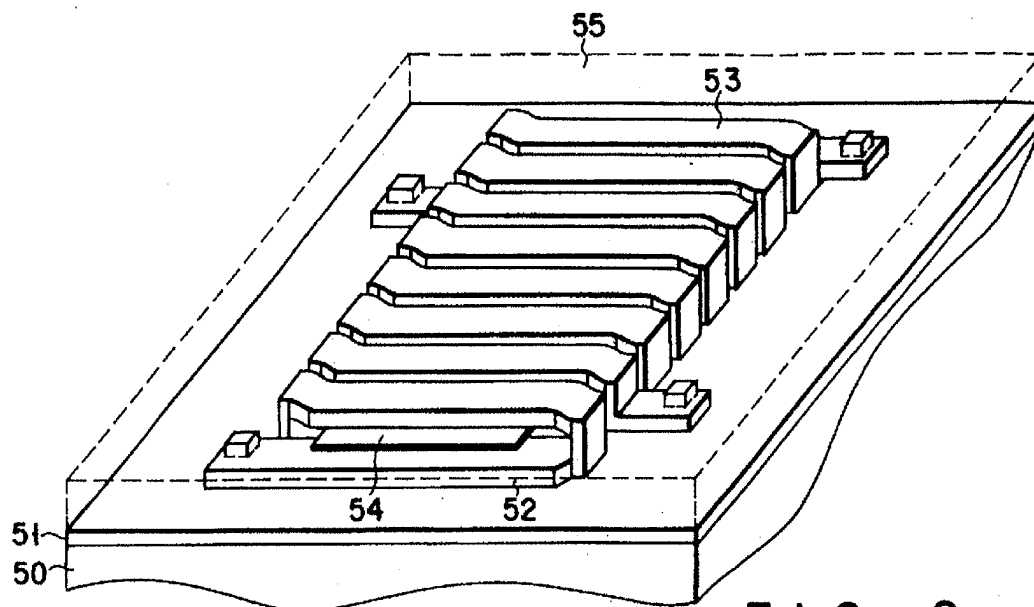


FIG. 9

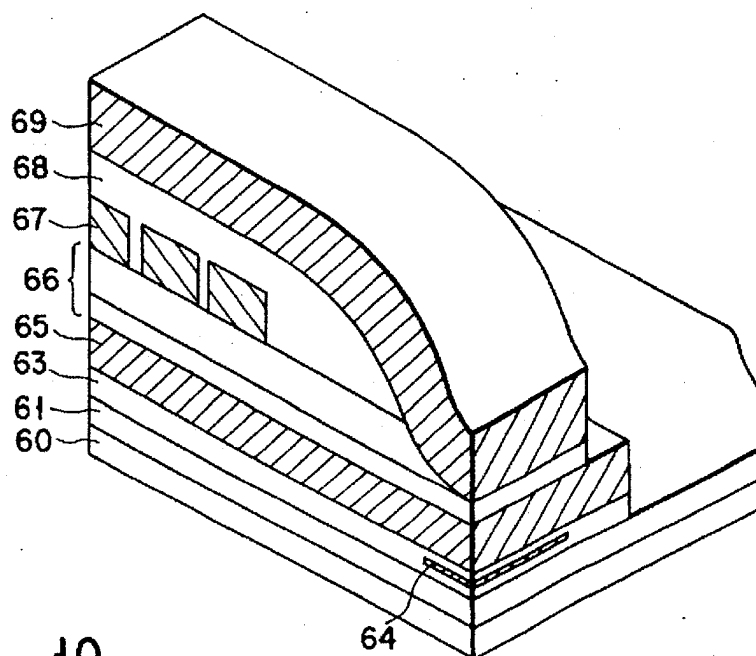


FIG. 10



US005851681A

United States Patent [19]

Matsuyama et al.

[11] **Patent Number:** 5,851,681[45] **Date of Patent:** Dec. 22, 1998

[54] **WIRING STRUCTURE WITH METAL
WIRING LAYERS AND POLYIMIDE
LAYERS, AND FABRICATION PROCESS OF
MULTILAYER WIRING BOARD**

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[73] Assignee: Hitachi, Ltd., Tokyo, Japan

[21] Appl. No.: 212,766

[22] Filed: Mar. 15, 1994

[30] **Foreign Application Priority Data**

Mar. 15, 1993 [JP] Japan 5-054318

[51] **Int. Cl.⁶** G11B 5/40; C08G 69/26

[52] **U.S. Cl.** 428/473.5; 428/209; 428/458;
428/694 ML; 174/258; 528/353

[58] **Field of Search** 428/209, 473.5,
428/615, 618, 458, 694 ML; 174/258

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Attorney, Agent, or Firm—Antonelli, Terry, Stout & Kraus, LLP

[57] **ABSTRACT**

This invention relates to a wiring structure having metal wiring layers and polyimide layers. An object of this invention is to overcome problems caused by oxidation of a metal surface, such as an increase in the resistance of wiring and a reduction in insulation, by preventing a reaction between a metal of the wiring layers, such as copper, and carboxyl groups of polyamic acid which make up the polyimide layers. In the wiring structure according to the present invention, the polyimide layers have been formed by heating and curing a resin composition which comprises a polyimide precursor, an amine compound and an organic solvent.

14 Claims, 1 Drawing Sheet

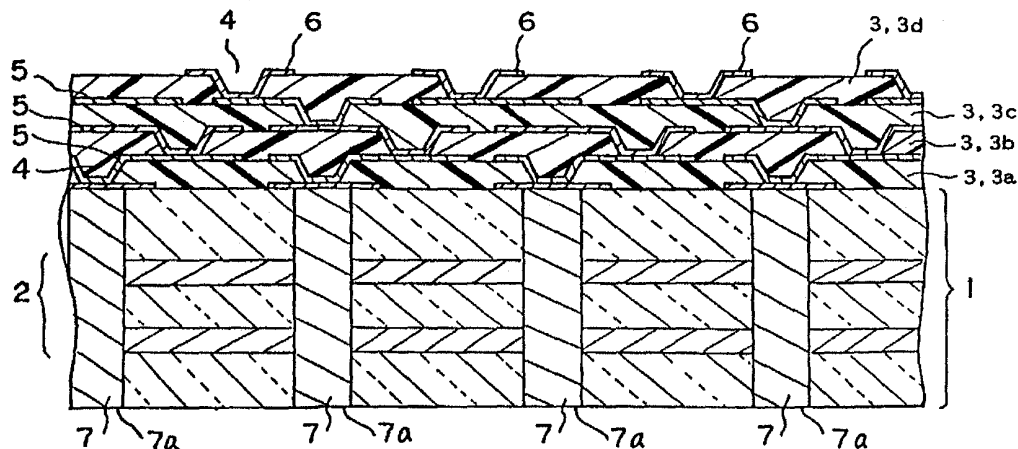


FIG. 5

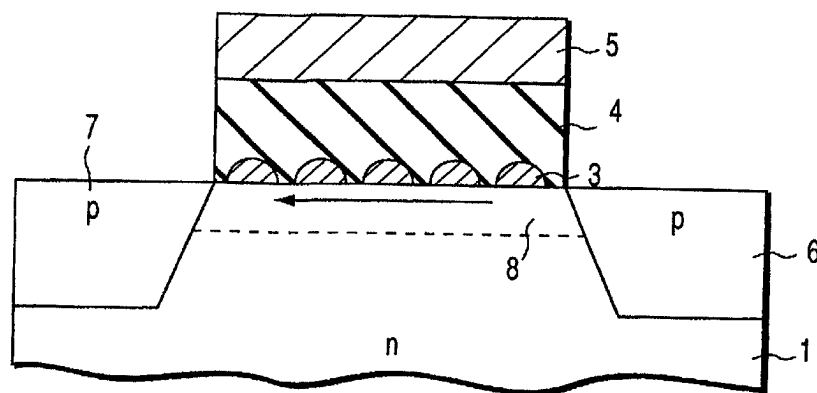


FIG. 6

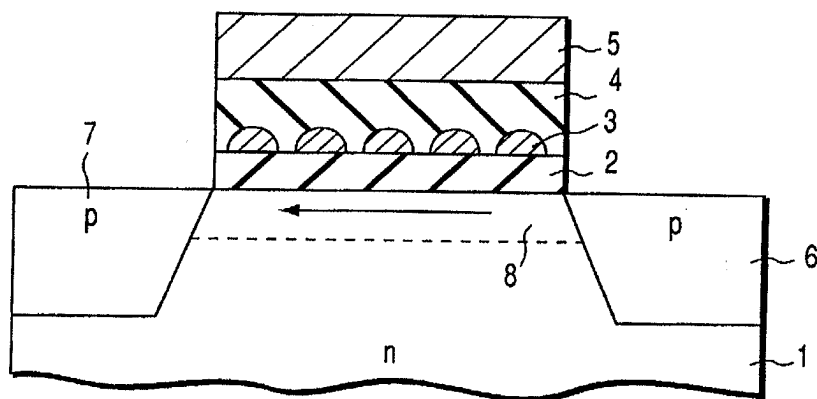


FIG. 7A

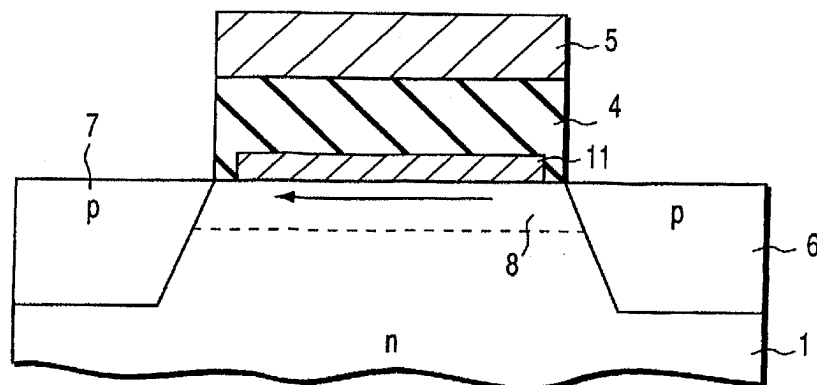


FIG. 3

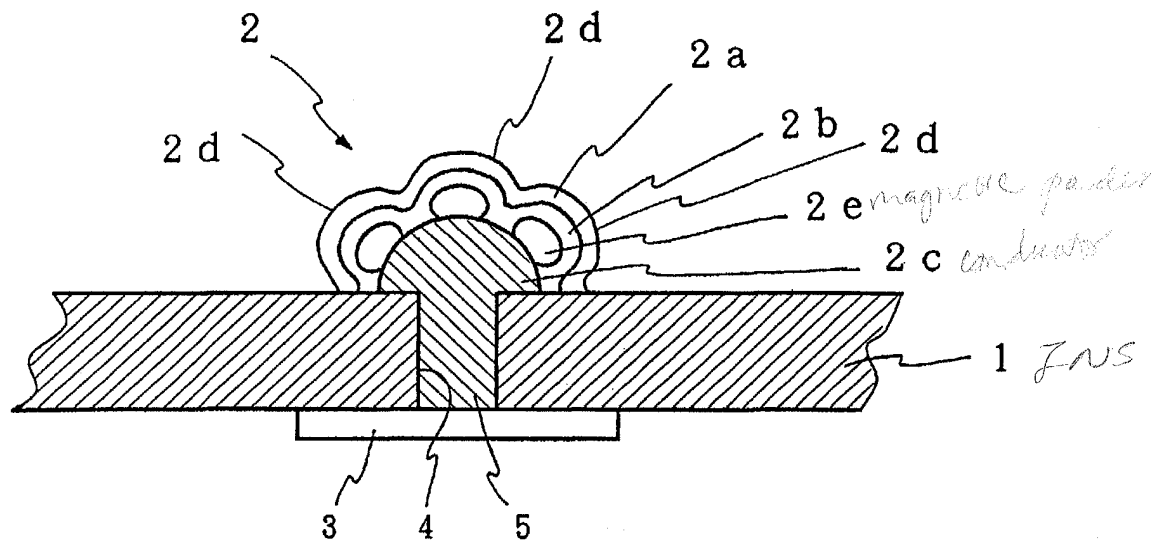
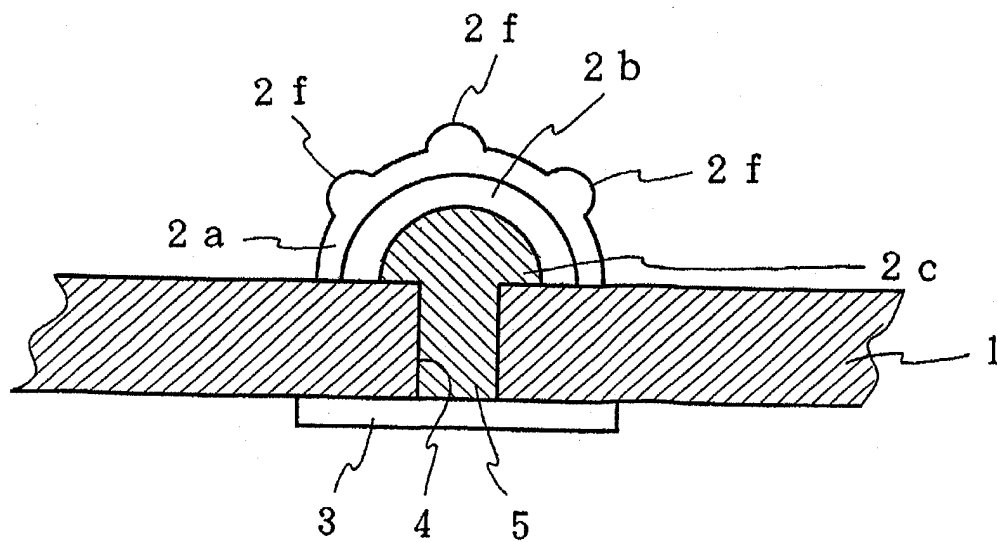


FIG. 4



Find what: magnetic

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Area: ☐ All ☐ Sel/Cur

Direction: ☐ Up ☐ Down

Match word: ☐ Whole ☐ Part ☐ Left ☐ Right

Look in: ☐ Grid ☐ Documents

☐ Match case

strip conductor 9 is formed on the lower surface of the dielectric layer 2B, the first MS line 8 is constituted by the interaction of the strip conductor 7 and the ground layer 6, and the second MS line 10 is constituted by the interaction of the strip conductor 9 and the ground layer 6.

DEPR:

An increase in the current just on the slot 11 results in an increase in the intensity of the magnetic field at this place, and a magnetic field is generated accompanied by an intense magnetic field encircling the strip conductor 7 of the MS line 8. Upon adjusting the length SL of the slot 11, therefore, an intense electromagnetic field is excited in the slot 11 due to the magnetic field generated by the MS line 8. Then, an electromagnetic field is generated even by the MS line 10 of the lower surface accompanied by an intense magnetic field which encircles the strip conductor 9, and high-frequency signals fed to the MS lines 8 are transmitted to the MS line 10 through the slot 11.

DEPR:

The magnetic field of high-frequency signals transmitted over the transmission line assumes an encircling form on a plane perpendicular to the MS line at all times unlike that of the case of when a via hole conductor is used, and migrates from the MS line 8 to the MS line 10 through the slot 11 in an

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Sep. 14, 1999

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FIG. 1

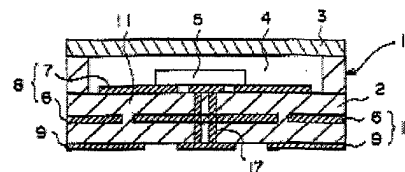
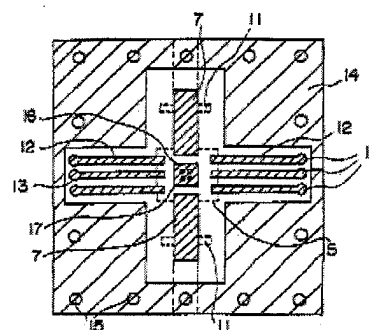


FIG. 2



Details Text Image

KWIC

Details Text Image

Full